PATENT SPECIFICATION 1,102,208

DRAWINGS ATTACHED.

1,102,208

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COMPLETE SPECIFICATION.

Transistor Bias Network.

We, MOTOROLA INC., a corporation of the State of Illinois, United States of America, of 9401 West Grand Avenue, Franklin Park, Illinois, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to a bias network for a semiconductor amplifier circuit and in particular to a transistor bias circuit incorporating a Darlington string and constructed in the form of a monolithic integrated circuit.

Transistor circuits are usually biased by the application of a desired bias voltage from resistor voltage dividers to the transistor. When the transistor is biased in this manner the bias current through the transistor is a function of the bias voltage, the voltage drops across the base emitter junctions of the transistors in the circuit and the resistance in series with the transistor bias current path. Since the transistor is essentially a current device, it is important that the bias current therethrough be maintained at a desired value, even though the characteristics of the transistors undergo large changes with changes in the ambient temperature. Since the voltage at the output of a resistor voltage divider circuit is essentially independent of the temperature, there is no compensation for the large changes in transistor characteristics with temperature. With conventional bias methods, the large changes in transistor characteristics over a wide temperature range will cause the voltage drop across the base emitter junctions to change to such an extent that extremely large changes in bias current will occur with changes in ambient temperature.

[*Price* 4*s.* 6*d.*]

In integrated circuit structures, the values of resistances available to the designer are limited and therefore a bias circuit may be coupled to active transistor electrodes through a semiconductor junction to maintain a high impedance at the electrode to which the bias circuit is coupled. The added junction necessary to couple the bias circuit to the active transistors increases the problem of maintaining the proper current flow through the transistors with changes in temperature since the voltage drop across the coupling semiconductor junction also changes with temperature in the same manner as the voltage drops across the base emitter junctions of the active transistors.

It is therefore an object of this invention to provide a bias circuit for use in a monolithic integrated circuit structure and which will maintain the desired bias current with changes in ambient temperature and transistor characteristics.

Another object of this invention is to provide a bias circuit for use in a monolithic integrated circuit structure and which will maintain a desired bias current through the transistors when the bias circuit is coupled to the transistors by a semiconductor junction.

A feature of this invention is the provision of a bias circuit for transistors formed in a monolithic integrated circuit structure and including a current supply coupled to a Darlington string for developing a bias potential of the proper value to produce desired bias currents to the transistor circuit.

According to the present invention there is provided a bias network for a semiconductor amplifier circuit, which amplifier circuit includes a plurality of semiconductor PN junctions connected in cascade between

an input bias terminal and an output terminal, the PN junctions of the amplifier circuit undergoing voltage changes with ambient temperature variations which tend to cause variations in current in the cascaded PN junctions of the amplifier circuit for a constant bias voltage at the input bias terminal, characterised in that the bias network includes a plurality of semiconductor devices having a corresponding plurality of cascaded PN junctions connected between the input bias terminal and a power supply and providing voltage changes with temperature variations which tend to offset the voltage changes with temperature variations of the PN junctions in the amplifier circuit thereby causing the voltage at the input bias terminal to change with temperature and the bias current to divide equally between the cascaded PN junctions in the amplifier circuit and the cascaded PN junctions in the bias network, maintaining a constant current in the amplifier circuit in the presence of ambient temperature variations.

The invention will now be described by way of example only with particular reference to the accompanying drawing wherein:

Figure 1 is a schematic diagram of an embodiment of the invention in which the bias circuit is coupled to a transistor amplifier circuit by means of a semiconductor junction;

Figure 2 is a schematic embodiment of a second embodiment of the bias circuit of Figure 1;

Figure 3 is a schematic of a circuit in which the bias circuit is coupled directly to the transistor amplifier, and

Figure 4 is a drawing showing the integrated circuit structure of the circuit of Figure 1.

In practicing this invention a bias circuit is provided for a monolithic integrated amplifier circuit. In one form of the circuit a pair of transistors are connected in series, with the emitter of the first transistor being connected to the base of the following transistor. The bias circuit consists of a Darlington string coupled to a constant current source with the number of transistors in the Darlington string being equal to the number of transistors in the amplifier circuit. A bias potential is produced at the input of the Darlington string which is a function of the betas and base-emitter potentials of the transistors, and the magnitude of the current in the Darlington string.

The potential developed at the input to the Darlington string is coupled to the amplifier circuit and will produce a current through the transistors in the amplifier circuit substantially equal to the current through the Darlington bias circuit. Since the circuits are formed as a monolithic integrated circuit structure the betas of the transistors are substantially equal and the current through the amplifier circuit will divide in the same manner as the current through the Darlington bias circuit. The transistors of the Darlington string also have the same temperature characteristics as the transistors in the amplifier circuit so that the voltage at the input to the Darlington bias circuit will automatically change to compensate for changes in the characteristics of the amplifier transistors to maintain the desired bias current through the active transistors.

In Figure 1, transistors 10 and 15 are coupled in series and form a video amplifier. Collector 11 of transistor 10 is coupled to a reference potential and collector 16 of transistor 15 is coupled to the same reference potential through resistor 24. Emitter 12 of transistor 10 is coupled to base 18 of transistor 15 and emitter 17 of transistor 15 is coupled to power supply 30 through resistor 28. Input terminal 20 is coupled to base 13 of transistor 10 through coupling capacitor 22 and output terminal 26 is coupled to collector 16 of transistor 15. The use of two transistors 10 and 15 cascaded in this manner provides an input impedance equal to $\beta^2_o R_o$ where R_o is the emitter resistor 28 and β_o is the beta of transistors 10 and 15. This provides means for developing a high input impedance which may be of the order of 500 K ohms in a typical circuit of this type. In operation, a positive video pulse is applied to input terminal 20 and is coupled to base 13 of transistor 10 through coupling capacitor 22. The pulse is amplified by transistor 10 and 15 and an output pulse is developed across resistor 24 and at output terminal 26.

In semiconductor devices manufactured in a monolithic integrated circuit form, it is difficult to build resistors having resistance values very much greater than 20 K ohms. Thus, if a bias circuit were to be coupled directly from the reference potential to base 13 through resistor 32 the input impedance to the circuit would be of the order of 20 K ohms which is very much less than the desired 500 K ohms input impedance. To eliminate this problem a semiconductor device 34, having base 35 and collector 36 coupled together to form a diode, is coupled to terminal point 40 to receive a bias potential. The development of this bias potential will be explained in a subsequent portion of this specification. Emitter 37 of diode 34 is coupled to base 13 of transistor 10. When a positive input pulse is applied to terminal 20, diode 34 is biased off so that the input impedance presented to the signal is maintained at a high value.

The bias voltage appearing across resistor 28 is equal to the bias voltage developed at terminal point 40 minus, the voltage drops across the base-emitter junctions of diode 34 and transistor 10 and 15. If the bias voltage at terminal point 40 were maintained at a constant value with changes in temperature, as would be the case with the normal voltage divider circuit, the changes in the voltage drops across diode 34 and transistors 10 and 15 would cause a large percentage change in the voltage across resistor 28 thus causing the bias current to undergo a large percentage change. In circuits of this type a conventional voltage divider circuit may be excepted to cause a 200% or more change in bias current with a change in temperature from −55°C to +125°C.

The magnitude of the bias voltage at terminal point 40 is established by a Darlington string consisting of transistor 42 having base 43 and collector 44 coupled together to form a diode and transistors 47 and 51. Emitter 45 of diode 42 is coupled to base 48 of transistor 47. Emitter 49 of transistor 47 is coupled to base 52 of transistor 51 and emitter 53 of transistor 51 is coupled to power supply 30. Collectors 50 and 54 of transistors 47 and 51 respectively are coupled to collector 44 of transistor 42.

In operation, resistor 32 and power supply 30 act as a current source for the Darlington string and diode 42. Thus, the current through diode 42 and the Darlington string is established at a desired value, independent of the characteristics of the transistors in the string. The transistors in the string divide the current between them according to the voltages across the individual transistors and the beta's of these transistors. The voltage across each transistor in the Darlington string is dependent upon the beta and the base-emitter junction potential of each transistor. The bias potential established at terminal point 40 is equal to the sum of the voltages across the base to emitter junctions of diode 42 and transistors 47 and 51. The potential at terminal point 40 will cause the same division of current through transistors 10 and 15 as the current division through transistors 47 and 51 so that transistors 10 and 15 will be properly biased.

Changes in the characteristics of transistors 42, 47 and 51 caused by changes in ambient temperature will cause the voltage at terminal point 40 to change so as to maintain the desired current flow through transistors 10 and 15. Thus, the bias current flowing through transistors 10 and 15 is substantially independent of the changes in the characteristics of these transistors with temperature and is dependent only upon the changes in the value of resistance 32 with temperature. Over the temperature range of from −55°C to +125°C this resistance may be expected to change 20% causing a 20% change in the bias current through transistors 10 and 15.

In the circuit shown in Figure 1 the bias current through transistors 10 and 15 will not be exactly equal to the current through the Darlington string since emitter 53 of transistor 51 is coupled directly to power supply 30 while emitter 17 of transistor 15 is coupled to power supply 30 through resistor 28. This difference in the bias currents, however, will be maintained across the temperature range of interest and can be used to develop bias potentials across transistors 10 and 15 which have desirable properties.

Use of resistor 28 in series with emitter 17 of transistor 15 causes less current to flow in transistor 15 than in the Darlington string. This amounts to class B biasing of the amplifier circuit. However, the input signal threshold level required to bring the amplifier circuit into the "active" region is not changed significantly while the use of class B bias results in a significant reduction in standby power consumption.

In Figure 2 a second embodiment of this invention is shown in which the portions of the circuit of Figure 2 which are identical to those of Figure 1 have the same reference numerals. In Figure 2 resistor 60 couples emitter 53 of transistor 51 to power supply 30. Resistor 60 can be made equal to resistor 28 whereby the current flow through transistors 10 and 15 is substantially equal to the current flow through the Darlington string. Resistor 60 may have other values so that a desired current will be developed to bias transistors 10 and 15.

In Figure 3 another embodiment of the invention is shown in which circuit elements identical to those of Figures 1 and 2 have the same reference numerals. In Figure 3 terminal point 40 is coupled directly to the base 13 of transistor 10. Thus, only a pair of transistors 47 and 51 are required in the Darlington string to provide the proper bias potential at terminal point 40. In addition, terminal point 40 is coupled to power supply 30 through a constant current source 62 to maintain a constant current through transistors 47 and 51. Constant current source 62 may be designed in a known manner to maintain a constant current through transistors 47 and 51 independent of the ambient temperature. By using a constant current source 62 to supply the current to the Darlington string the bias current through transistors 10 and 15 can be maintained substantially constant over a large temperature range.

In Figure 4 is a drawing of the physical structure and layout of the circuit of Figure

1 manufactured in a monolithic integrated circuit form. The portions of the structure of Figure 4 which represent components of Figure 1 in an integrated form the characteristics of the transistors can be made to match very closely, thus providing excellent control of the bias current with changes in ambient temperature.

Thus, a bias circuit has been shown which is readily adaptable to manufacture in a monolithic integrated circuit form. The circuit provides the correct bias current for a transistor circuit and compensates for changes in ambient temperature. The bias circuit can be coupled to the transistor circuit by a diode so that the input impedance of the transistor circuit is maintained at a high level. Resistance may be inserted in series with the transistor circuit to cause class B operation with low standby bias current requirements.

WHAT WE CLAIM IS:—

1. A bias network for a semiconductor amplifier circuit, which amplifier circuit includes a plurality of semiconductor PN junctions connected in cascade between an input bias terminal and an output terminal, the PN junctions of the amplifier circuit undergoing voltage changes with ambient temperature variations which tend to cause variations in current in the cascaded PN junctions of the amplifier circuit for a constant bias voltage at the input bias terminal, characterised in that the bias network includes a plurality of semiconductor devices having a corresponding plurality of cascaded PN junctions connected between the input bias terminal and a power supply and providing voltage changes with temperature variations which tend to offset the voltage changes with temperature variations of the PN junctions in the amplifier circuit thereby causing the voltage at the input bias terminal to change with temperature and the bias current to divide equally between the cascaded PN junctions in the amplifier circuit and the cascaded PN junctions in the bias network, maintaining a constant current in the amplifier circuit in the presence of ambient temperature variations.

2. A bias network as claimed in Claim 1 characterised in that a resistor is connected between the power supply and the input bias terminal to establish a current through the cascaded PN junctions of the bias network.

3. A bias circuit as claimed in Claim 2 characterised in that a first diode is connected between the input bias terminal and the plurality of semiconductor devices, a second diode connects the input bias terminal to the input of the amplifier circuit and the first diode compensating for the voltage drop across the second diode.

4. A bias network as claimed in Claim 1 characterised in that a constant current supply is connected between the power supply and the input bias terminal to provide a current to the cascaded PN junctions in the amplifier circuit and the bias network.

5. A bias circuit as claimed in Claim 1 characterised in that the plurality of cascaded PN junctions in the bias network are formed by transistors in a Darlington string connection between the power supply and the input bias terminal, and a current limiter resistor connected between the amplifier circuit and the power supply.

6. A bias network as claimed in Claim 1 characterised in that the plurality of cascaded PN junctions are formed by a plurality of transistors connected as a Darlington string with a first transistor of the string having its base and collector electrodes connected together at the input bias terminal to form a first semiconductor diode, a first resistor connected between the amplifier circuit and the power supply, a second resistor connected between the output electrode of the final transistor in the Darlington string and the power supply, a source of constant current connected between a point of reference potential and the input bias terminal to supply current to said Darlington string and to said amplifier circuit, and a second semiconductor diode connected between the input to the amplifier circuit and the input bias terminal, and the first semiconductor diode compensating for voltage variations with temperature in the second semi-conductor diode.

7. A bias network as claimed in Claim 1 characterised in that the plurality of cascaded PN junctions therein are formed by a pair of transistors in a Darlington string connection with a first of said pair of transistors connected collector-to-base at the input bias terminal to form a semiconductor diode, a first resistor connected between the amplifier circuit and the power supply, a second resistor connected between the output electrode of the second of said pair of transistors and the power supply, and a constant current source connected between the power supply and the input bias terminal to provide a current to said Darlington string and to said amplifier circuit.

8. A bias circuit for a semiconductor amplifier circuit substantially as hereinbefore described and as shown in the accompanying drawing.

For the Applicants:
F. J. CLEVELAND & COMPANY,
Chartered Patent Agents,
Lincoln's Inn Chambers,
40/43 Chancery Lane, London, W.C.2.

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1102208 COMPLETE SPECIFICATION

1 SHEET *This drawing Is a reproduction of the Original on a reduced scale*

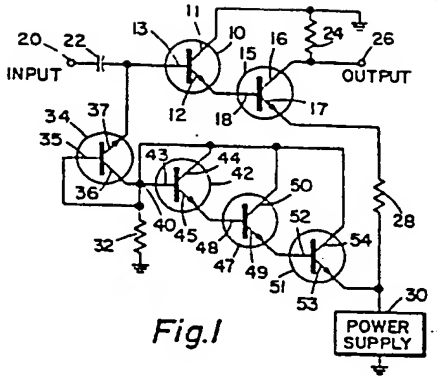

Fig.1

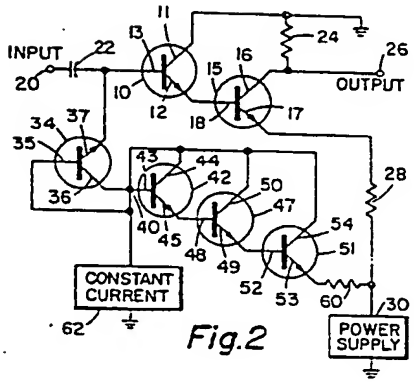

Fig.2

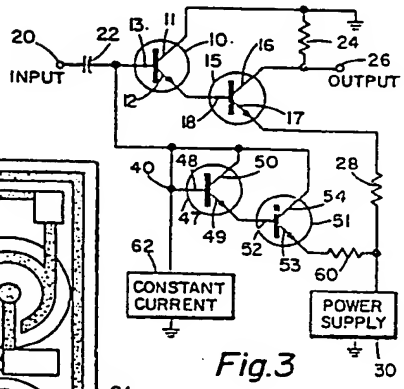

Fig.3

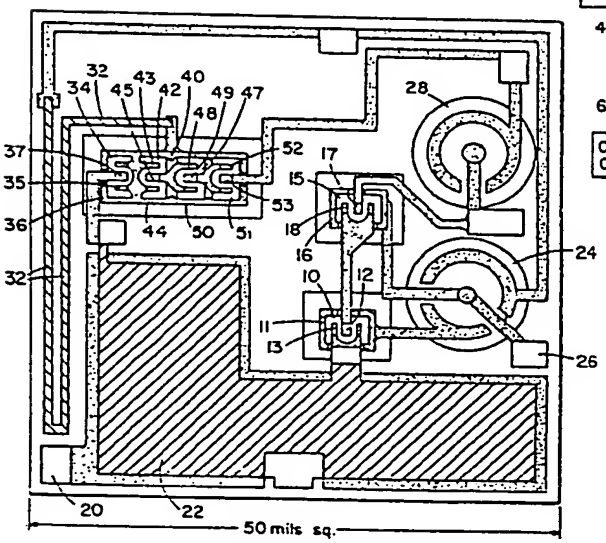

Fig.4